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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,106	08/23/2001	James M. Derderian	4832US (01-0104)	1038

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TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER

IM, JUNGHWAM

ART UNIT	PAPER NUMBER
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2811

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

09/938,106

Applicant(s)

DERDERIAN, JAMES M.

Examiner

Junghwa M. Im

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 November 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 23-27,29-35,40-51 and 53-64 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 23-27,29-35,40-51 and 53-64 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 23 and 45 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 23 and 45 recite that the back side of the second semiconductor device, that is, the weight of the second semiconductor device is supported “entirely” by the discrete elements (the wires). Note that the instant invention does not show this aspect. Rather, the figures of the instant invention show that the second (upper) semiconductor device is supported collectively by other elements under the second semiconductor device such as the wires and the adhesive layer through forming a complete package.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 23 and 45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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Claims 23 and 45 recite that the discrete elements supports “entirely” the back side of the semiconductor device and it is confusing to understand how the discrete elements (wires) can support the entire weight of the semiconductor device since this aspect is not disclosed in the instant invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 23, 24, 29, 30, 33, 40, 45, 46, 49, 50, 53, 59 and 61-64 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. (US 6400007), hereafter Wu.

Regarding claims 23 and 45, insofar as understood, Fig. 4 of Wu shows a device to use a method for assembling semiconductor devices with a densely stacked arrangement (col.2, line 64 through col. 3, line 61), comprising;

a first semiconductor device 28;

discrete conductive elements 32 over portions of said first semiconductor device and;

positioning a second semiconductor device 34 over the first semiconductor device, a back

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side of the second semiconductor device resting upon at least some of discrete conductive elements and being supported by being electrically isolated from each other (col.3, lines 54-56).

Regarding the limitation of “a back side of the second semiconductor device ... being supported thereby,” Fig. 5 of Wu shows that the discrete conductive elements (the wires) contributes to support the back side of the second semiconductor device with adhesive layers (50, 52) since the wires are in the direct contact beneath the back side of the second semiconductor device. In addition, Examiner would like to point out that the second (upper) semiconductor device is supported *collectively* by other elements under the second semiconductor device such as the wires and the adhesive layer through forming a complete package. Note that even the lower (first) semiconductor contributes a part of the collective support for the upper semiconductor device. That is, all elements connected directly or indirectly to one another is “collectively support one another.”

Regarding the limitation in the preamble of claim 45, Fig. 4 of Wu shows “semiconductor device in a stacked arrangement with stacked arrangement having a height substantially equal to combined thickness of each of the semiconductor device and distances discrete conductive elements associated therewith protrude above said each of the semiconductor devices.” In addition, note that the limitation in the preamble does not have patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951).

Regarding claims 24 and 46, Wu discloses positioning the second semiconductor

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device comprises positioning the second semiconductor device on said at least some of discrete conductive elements with the back side and the discrete conductive elements in mutual electrical isolation (col.3, lines 54-56).

Regarding claims 29 and 49, Wu discloses a quantity of adhesive material 50 to at least an active surface of the first semiconductor device (col.3, lines 24-25).

Regarding claims 30 and 50, it is inherent that the device of Wu shows drawing the second semiconductor device toward the first semiconductor device after applying the adhesive on the first device since the adhesive is applied on the active surface of the first semiconductor device and positioning the second semiconductor device is followed.

Regarding claims 33 and 53, it is inherent that the applying includes applying the quantity of the adhesive material after positioning the second semiconductor device since the second semiconductor device will be stacked on top of the first semiconductor device by the adhesive.

Regarding claims 40 and 59, Wu discloses securing the first semiconductor device and a substrate to one another (col.3, lines 16-20).

Regarding claim 61, it is inherent that electrical communication would be established between bond pads of the second semiconductor device (34) and the corresponding contact areas of the substrate (col. 3, lines 41-43) in order to have the device operate functionally.

Regarding claim 62, Fig. 4 of Wu shows establishing communication comprises placing additional discrete conductive elements (56; wires) between each of the bond pads and the corresponding contact area of the corresponding contact areas.

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Regarding claim 63, Fig. 4 of Wu shows providing at least one connective element (42; signal output terminal) in communication with at least one bond pad of each of said first and second semiconductor devices (col. 3, lines 4-8).

Regarding claim 64, Wu discloses a method further comprising encapsulating (58 in Fig. 4; a packaging layer) said first and second semiconductor devices (col. 3, lines 44-47).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 25, 26, 31, 34, 35, 41-44, 47, 51, 54-58 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable under obviousness over Wu in view of Lee et al. (US 6,388,313), hereafter Lee.

Regarding claims 25 and 47, Wu discloses the most aspect of the instant invention except “providing a dielectric coating on at least portion of said discrete conductive elements.” Lee discloses a method providing a dielectric coating on at least portion of said discrete conductive elements (col. 5, lines 40-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to apply a coat on the discrete conductive elements (wires) of Wu’s device with the teaching of Lee in order to prevent a short circuit between the semiconductor device and the bare wires.

Regarding claim 26, Lee shows a method wherein the providing comprises forming at least one of a dielectric oxide and a dielectric polymer coating on at least said portions of the discrete conductive elements (col. 5, lines 22-24).

Regarding claims 31 and 51, Wu does not disclose “said drawing is effected by at least one of capillary action of the adhesive material, curing of the adhesive material, application of heat to the adhesive material, and vibration of the adhesive material.” However, it would be obvious that such drawing is effected by one of the effects recited by the pending claim since Wu’s adhesive material (resin) is identical to the one recited in the instant invention. Furthermore, Lee discloses the drawing is effected by at least curing of the adhesive material (resin) and application of heat to the adhesive material (curing; col. 5, lines 32-40).

The limitations regarding claims 34 and 35 have been discussed in claims 30 and 31 with the combined teaching of Wu and Lee.

Regarding claim 41, Wu does not disclose “said placing the discrete conductive elements comprises securing the discrete conductive elements to contact areas of the substrate and the bond pads of the first semiconductor device.” Lee shows a method wherein the placing the discrete conductive elements comprises securing the discrete conductive elements to contact areas of the substrate and the bond pads of the first semiconductor device (col. 5, lines 8-10). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Lee into the device of Wu in order to have signals transferred between the stacked devices through having the discrete conductive elements (wires) secured on the contact areas (bond pads) on the substrate.

Regarding claim 42, Lee shows the securing comprises electrically connecting bond pads of the second semiconductor device to the corresponding contacts areas of the substrate (col. 5, lines 13-16).

Regarding claim 43, Lee shows encapsulating at least portion of at least one of the substrate, the first semiconductor device, and the second semiconductor device (col. 6, lines 32-36).

Regarding claim 44, Lee shows forming external conductive elements 27 in Fig. 1 on the substrate in electrical communication with corresponding contact areas (col. 5, lines 1-4).

Limitations of claims 54 and 55 have been discussed in claims 34 and 35.

Regarding claim 56, Wu fails to disclose “biasing at least one of the first and second semiconductor devices toward the other of the first and second semiconductor devices.” Lee shows biasing at least one of the first and second semiconductor devices toward the other of the first and second semiconductor devices (col. 4, lines 54-68). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Lee into the device of Wu in order to have an electrical connection for a necessary circuit configuration of the device.

Regarding claim 57, Lee shows controlling the biasing by means of adhesive (col. 4, lines 54-68).

Regarding claim 58, Lee shows the controlling the biasing comprises controlling the biasing force to a level sufficient to deform, kink, bend, or collapse the discrete conductive elements.

See the respective portions of the specification such as col. 5, lines 24-32.

Regarding claim 60, Wu fails to show “connecting the discrete conductive elements to corresponding contact areas of the substrate.” Lee shows connecting the discrete conductive elements to corresponding contact areas of the substrate (col. 5, lines 8-10). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Lee into the device of Wu in order to have current flow from supply contact areas of the substrate to the semiconductor devices through the discrete conductive elements (wires).

Claims 27, 32 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable under obviousness over Wu in view of Shim et al. (US 6,531,784), hereafter Shim.

Regarding claims 27 and 48, Wu does not disclose positioning a dielectric layer at least portions of the backside of the second semiconductor device. Fig. 7 of Shim shows the dielectric layer (50C) on the portion of the backside of the second semiconductor device. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Shim into the device of Wu in order to enhance the electrical isolation between the devices and the wires.

Regarding claim 32, Wu does not disclose positioning a dielectric layer at least portions of the backside of the second semiconductor device. Fig. 3 of Shim shows the dielectric layer (44) on the portion of the backside of the second semiconductor device. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Shim into the device of Wu in order to mount two devices securely.

Response to Arguments

Applicant's arguments filed November 13, 2006 have been fully considered but they are not persuasive. The rejection stands, modified only to accommodate the amendments made to the claims by Applicant. New rejections are made in response to Applicant amended claims. In addition, the examiner presents the remarks below in response to Applicant's arguments.

Applicant argues that "Final rejections of claims 23-27, 29-35, 40-51, and 53-64 were affirmed in the Decision. Independent claims 23 and 45 have been amended to place them in condition for allowance." It appears that the amendment is made to overcome the prior art referred in the Examiner's Answer and the subsequent Board's affirmation. As discussed above in the Office Action, the instant invention does not disclose that the entire back of the second (upper) semiconductor supported by the wires. Rather, the figures of the instant invention show that the second (upper) semiconductor device is supported collectively by other elements such as the wires and the adhesive layer through forming a complete package. Furthermore, one of ordinary skill in the art readily understands that the wires alone cannot hold the weight of the semiconductor device.

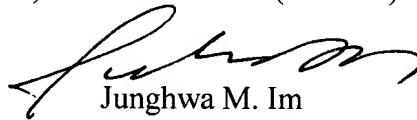
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Junghwa M. Im
Examiner
Art Unit 2811

jmi